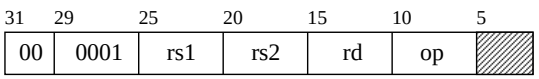
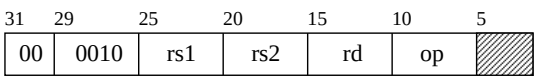
TinyISA rrr instruction format



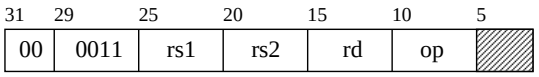
ArithOp

00000	ADD
00001	ADDU
00010	SUB
00011	SUBU
00100	MUL
00101	MULU



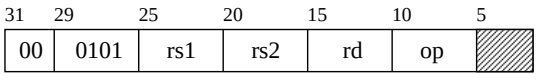
LogicOp

00000	AND
00001	OR
00010	XOR
00011	NAND
00100	NOR
00101	XNOR
00011	NOT
00100	LSL
00101	LSR
00110	ASR



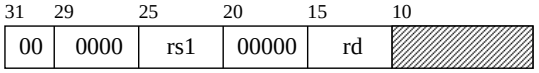
SetOp

00000	SEQ
00001	SNE
00010	SLT
00011	SLTU
00100	SLE
00101	SLEU
00110	SGT
00111	SGTU
10000	SGE
10001	SGEU

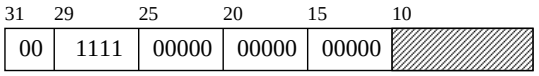


MEMop

00000	LDW
00100	STW

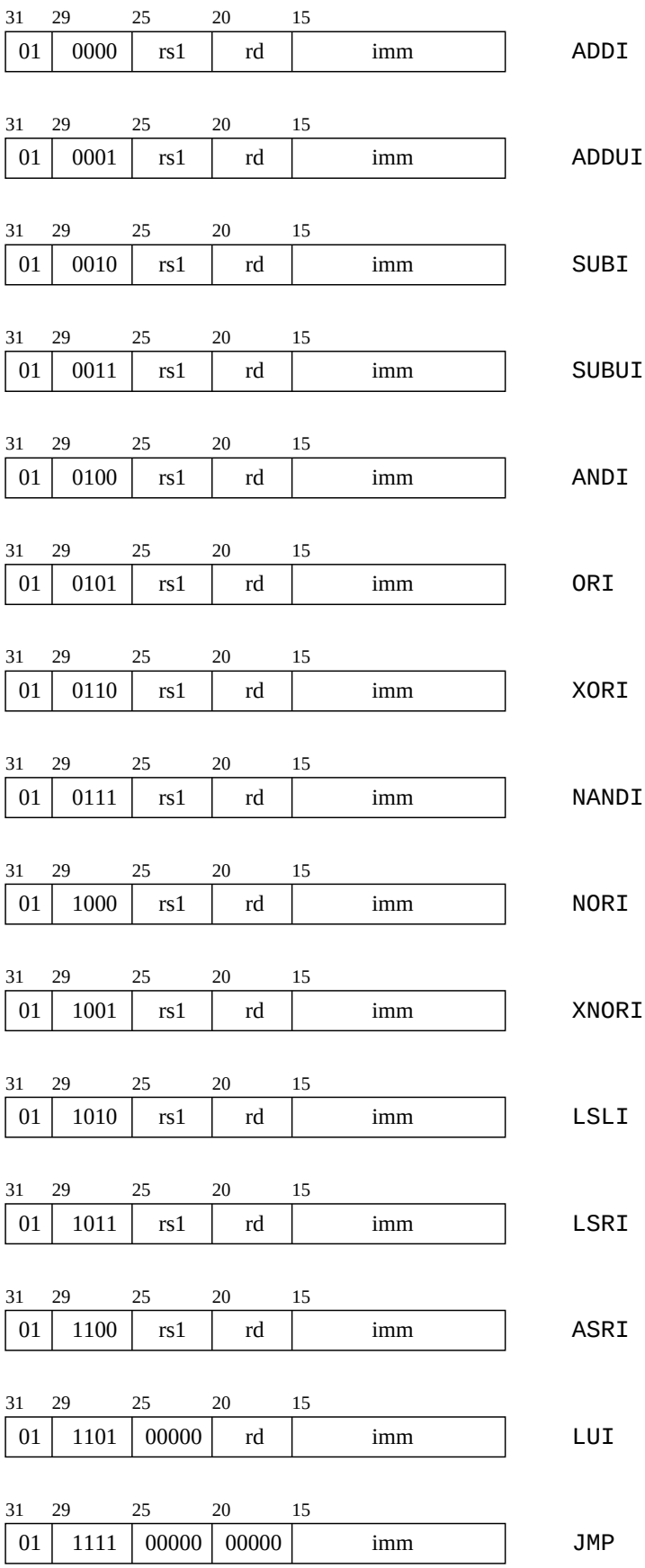


JMPL

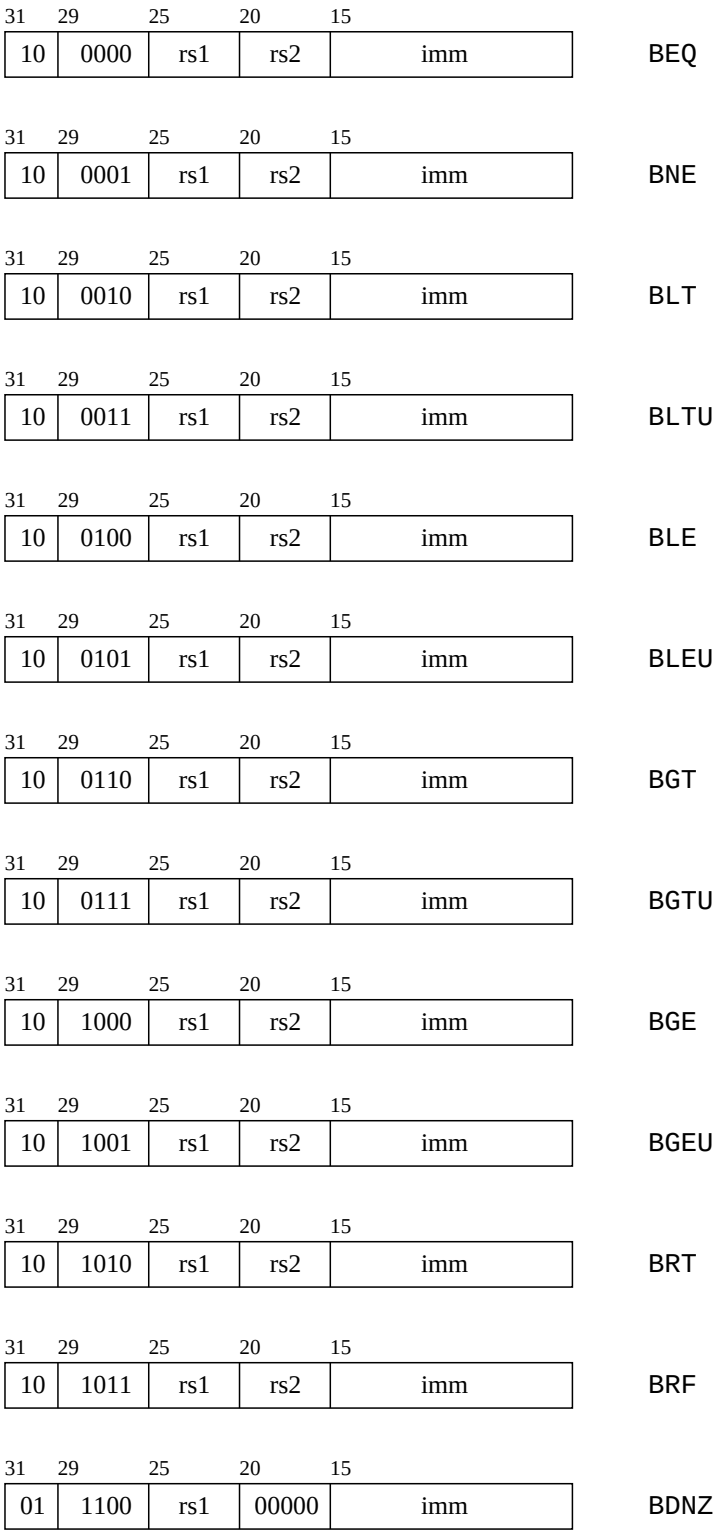
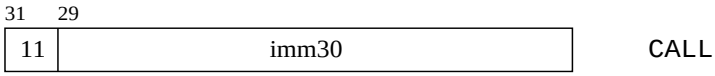


RET

TinyISA rr-imm instruction format



TinyISA branch instruction format



TinyISA CALL instruction format